25.7 An 11b 800MS/s Time-Interleaved ADC with Digital Background Calibration

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The upcoming 10GBase-T standard (IEEE 802.3an) offers 10Gb Ethernet over twisted-pair cabling. The receiver requires a wide dynamic range to accommodate the large echo and crosstalk interference. In such a receiver, the ADC requirements are a sampling rate of 800MS/s and a bandwidth of 400MHz with an ENOB > 9b. A time-interleaved ADC is suitable for this application [1]. The proposed ADC (Fig. 25.7.1) consists of a single T/H circuit, 4 interleaved pipelined sub-ADCs, digital calibration logic, reference-voltage buffers, and a clock generator. To reduce the power and area, an opamp-sharing technique is applied to sub-ADC pairs 0, 2 and 1, 3. Each sub-ADC consists of twelve 1.5b/stage MDACs to generate 13b outputs with 2 extra bits for calibration. The T/H and the sub-ADCs sample at 800 and 200MHz, respectively. The single T/H eliminates the timing skew and bandwidth mismatches that would arise from separate sampling networks [2]. The gain and offset mismatches between sub-ADCs are reduced by the digital background calibration.

The simplified schematic of the T/H is shown in Fig. 25.7.2. The circuit comprises a sampling network and a source follower. The sampling network employs a bootstrapped switch to reduce signal-dependent charge injection and increase the linearity and bandwidth in the track mode. The linearity of the source follower is degraded by body effect and channel-length modulation [3]. However, by tying the bulk of M1 to a duplicate output signal, the body effect can be eliminated. Transistor M2 acts as a cascode source-follower to produce this duplicate signal. It also keeps the V_{ds} of M1 constant, thus suppressing channel-length modulation. The threshold-voltage difference between M1 and M2 must be large enough to allow M1 to operate in the saturation region. Another advantage of this configuration is that the parasitic diode capacitance in the bulk of M1 is driven by M2 rather than M1 itself, thus improving the transient response of the source follower.

For correct operation of the MDAC and to maximize the time budget for it to settle, the rising edge of the 800MHz sampling clock must fall in the non-overlap period. The phase skew caused by the divided-by-4 circuit and the non-overlapping clock generator is calibrated by a DLL. The clock jitter induced by the DLL and the non-overlap clock generator is not critical, because the sampling phase of the T/H is determined by the 800MHz clock, whose delay from the input clock buffer to the T/H is minimized.

Two reference voltage buffers are realized on chip. One voltage buffer drives sub-ADC0 and sub-ADC2 while the other drives sub-ADC1 and sub-ADC3. Instead of a conventional opamp-based feedback amplifier, an open-loop source follower is used as the voltage buffer, thus reducing power consumption and achieving fast settling. A replica bias is applied to the source follower to prevent the PVT variations of the reference output. However, even with careful and fully symmetric layout of the 2 voltage buffers, any reference level mismatch still translates to a gain mismatch between sub-ADCs. Experimental results show a 0.57% gain mismatch on average, which is corrected by the calibration procedure.

In the design of digital calibration algorithms, the statistic characteristics of 10GBase-T signal is exploited to reduce complexity while maintaining nearly no-loss ENOB performance [4]. Methods that are 10GBase-T data-aided have been proposed in [5]. However, algorithms proposed in this work do not rely on input data and operate as follows. The digital calibration circuit consists of 4 calibration sub-blocks for each sub-ADC that operates at 200MHz, and one MUX circuit that operates at 800MHz (Fig. 25.7.1). The 4 calibration sub-blocks separately receive the sampled data from sub-ADC0 to sub-ADC3, and subsequently estimate the gain and offset errors of sub-ADC1 to sub-ADC3 versus sub-ADC0. Finally, they apply the results to the MUX to produce a new time-interleaved output. The calibration sub-block is shown in Fig. 25.7.3. The upper and lower loops perform offset and gain calibration, respectively. The offset loop incorporates accumulate and average (acc&avg) circuits to estimate and track the DC values of the sub-ADCi output. The circuits calculate only one estimated DC value for each N-sample block. The LMS block compares the estimated DC values of sub-ADCi with sub-ADC0, or just with '0' if the input signal is DC-free. The error signal, e_{bi}, is then applied to update LMS offset values (b_i). The gain loop is similar, but it uses the absolute values of the correction-circuit output as input to the acc&avg circuit to estimate the gain error a_i. The correction circuit uses the estimated a_i/b_i to cancel gain and offset errors, producing a corrected sampled signal.

In order to prevent wrong tracking, foreground (power-up) calibration is performed first, to estimate initial values for the gain/offset by configuring the circuit as shown in Fig. 25.7.4. Following calibrations are performed sequentially and independently: (1) offset, (2) negative gain, and (3) positive gain calibration. During foreground offset calibration, a DC voltage V_{GND} is applied to all sub-ADCs and only the offset loop is turned on to estimate the offset error (Fig. 25.7.4(a)). During positive- and negative-gain calibration cycles, a reference voltage V_{ref_cal} (±0.45V) is applied to all sub-ADCs. In this case, only the gain loop estimates the gain error. During foreground gain calibration, the circuit applies previously estimated offset errors to the correction circuits (Fig. 25.7.4(b)).

During background calibration, both gain and offset loops are turned on to track drifting-errors (Fig. 25.7.3). If an input signal (10GBase-T or sine-wave) exists, the circuit tracks both residual errors and voltage/temperature variations. Measurement results show that this algorithm achieves nearly lossless performance.

The ADC is implemented in a 90nm CMOS technology, and the active area is 1.4mm^2. The digital calibration circuit occupies 0.7×0.3mm^2. The digital testing circuit, including an 8192×13b SRAM occupies an area of 0.7×0.5mm^2 for recording 800MHz real-time ADC samples or corrected signals. The total digital circuit consumes ~12mW. At a sampling rate of 800MHz, the DNL and INL are < 0.5LSB and 1.6LSB, respectively. In Fig. 25.7.5, the upper part shows the performance of the interleaved ADCs without and with calibration. The SNDRs after calibration are 58 and 54dB for 15 and 400MHz inputs, respectively. The lower part shows a comparison between sub-ADCs and the interleaved ADC with calibration. The performance of the calibrated ADC approaches the worst performance of 4 sub-ADCs. Figure 25.7.6 shows the output spectra without and with calibration when the sampling rate is 800MHz and the input frequency is 205MHz. Both the gain and offset are improved by 24dB. The HD_2 and HD_3 are less than -75 and -71dB, respectively. The measured dynamic range is 66dB and the estimated jitter calculated from the measured SNR of the ADC is <0.43ps. With a 1.3V supply voltage (1.5V for T/H), the ADC consumes 350mW (including the calibration logic). The micrograph is shown in Fig. 25.7.7.

References:

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[3] K. Hadidi, A. Khoei, "A Highly Linear Cascode-Driver CMOS Source-Follower Buffer," *IEEE Intl. Conf. on Electronics, Circuits and Systems*, pp. 1243-1246, Oct., 1996.
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[5] C. L. Lin, "Receiver Capable of Correcting Mismatch of Time-Interleaved Parallel ADC and Method Thereof," *U.S. patent pending App. no. 11/164491,* Nov. 25, 2005.

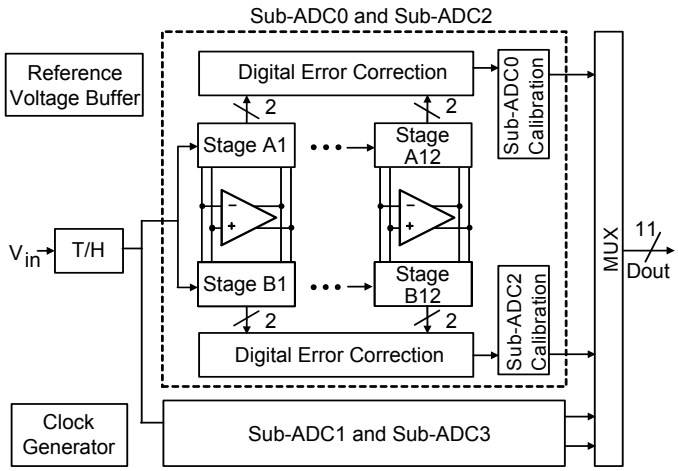

Figure 25.7.1: Block diagram of the ADC.

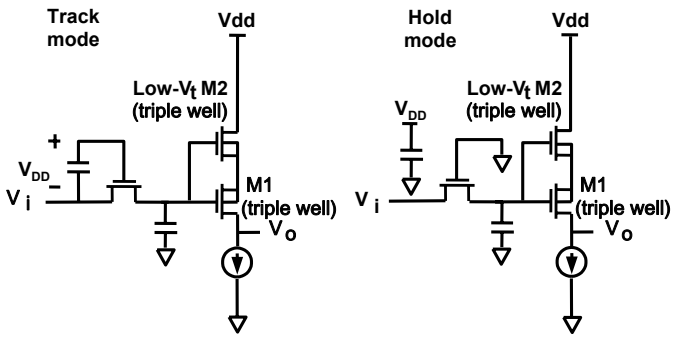

Figure 25.7.2: Track-and-hold circuit.

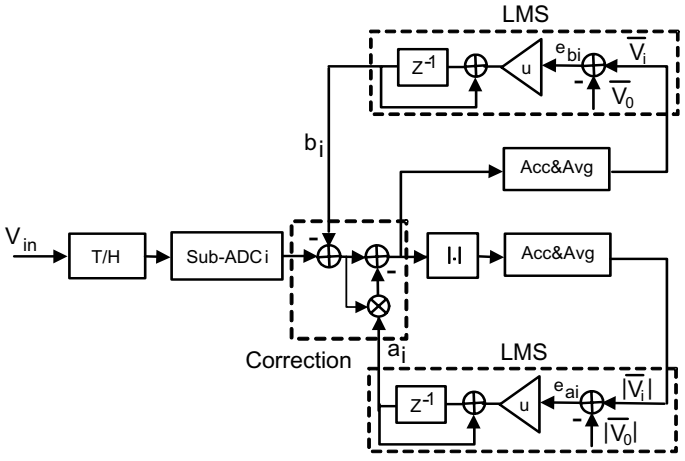

Figure 25.7.3: One sub-ADCi calibration block and background calibration configuration.

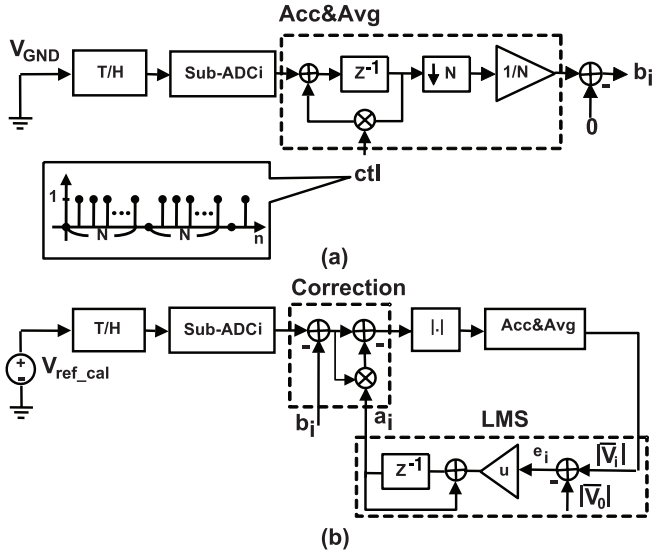

Figure 25.7.4: Foreground calibration configurations: (a) offset error (b) gain error.

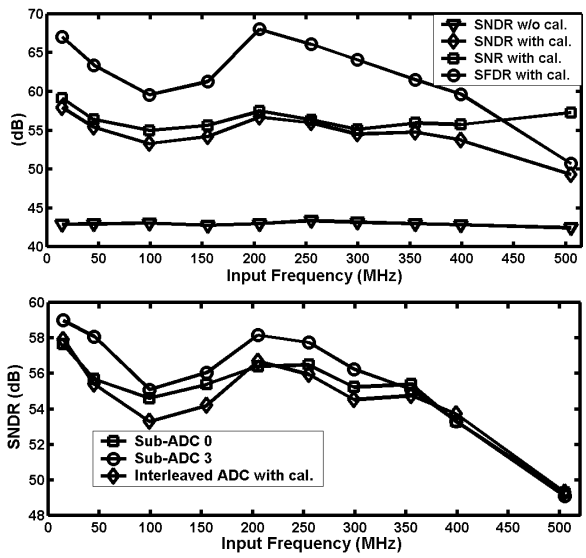

Figure 25.7.5: Measured dynamic performance.

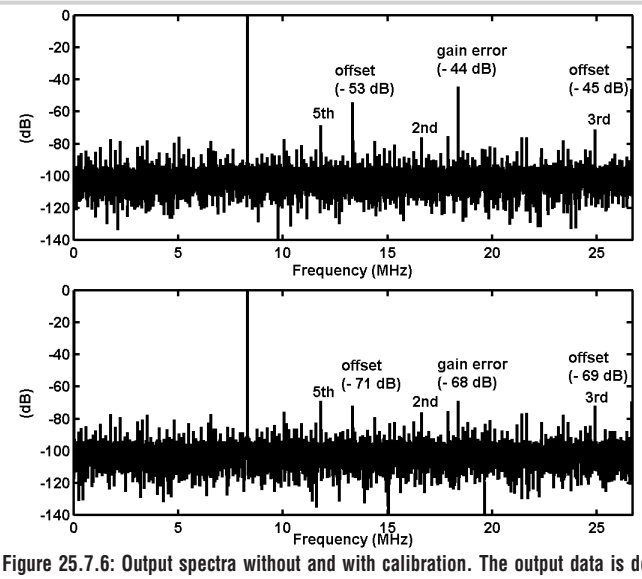

Figure 25.7.6: Output spectra without and with calibration. The output data is down-sampled by a factor of 15.

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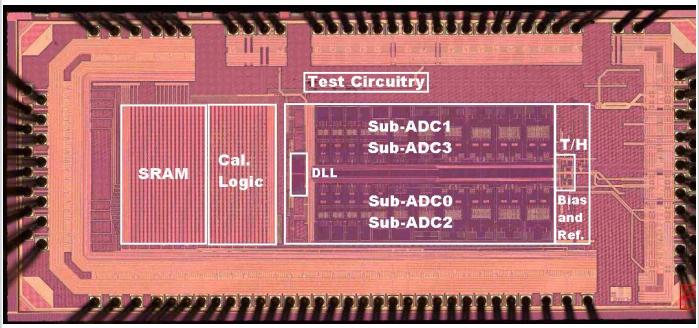

Figure 25.7.7: Die micrograph.

